

LESSON PLAN

Period	Date (tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	16/10/13	Review of NUSO electronics	I	Blackboard		
		MOS, CMOS, Bipolar Technology trends	"	"		
2	16/10/13	Lithography oxidation	"	"		
3	17/10/13	Ion Implantation metallization and	"	"		
		Diffusion Techniques	"	"		
4	20/10/13	$I_{ds} - V_{ds}$ Relationship	"	"		
5	20/10/13	Threshold Voltage V_{th}	"	"		
		Transconductance g_m & W/L	"	"		
6	24/10/13	Pass transistors	"	"		
		MOS, CMOS & BiCMOS Inverters	"	"		
7	30/10/13	$2m / \lambda_{pd}$ Relation	"	"		
8	31/10/13	MOS transistor Circuit Model	"	"		
		Latch-up in CMOS circuits	"	"		
9	1/11/13	Introduction to layout design & tools	II	"		
		Transistor structure	"	"		
10	2/11/13	wires and vias	"	"		
		Scalable Design rules	"	"		
11	6/11/13	Layout Design tools	"	"		
		Introduction logic Gates & Layout	"	PPT		
12	7/11/13	Static Complementary gates	"	"		

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13	8/11/13	Switch logic	II	PPT		
		Alternative gate circuits	"	"		
		Low Power Gates	"	"		
		Resistive and inductive	"	"		
14	9/11/13	Inductive interconnect delays	"	"		
		Introduction to Combinational logic networks	III	Blackboard		
15	11/11/13	Logic networks	"	"		
16	15/11/13	Logic gates	"	PPT		
		Simulation	"	"		
17	16/11/13	Network delay	"	"		
		Interconnect Design	"	"		
18	21/11/13	Power optimisation	"	"		
19	22/11/13	Switch logic networks	"	"		
20	23/11/13	Gates & network testing	"	"		
21	28/11/13	Introduction to sequenced systems memory cells & Arrays	IV	"		
22	29/11/13	Clocking discipline	"	"		
23	30/11/13	One phase & two phase	"	"		
24	7/12/13	Clocking system	"	"		

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		System Design	IV	PPT		
25	6/11/13	Power optimization	"	"		
		Design validation	"	"		
26	7/1/13	Sequential testing	"	"		
27	8/1/13	Introduction to floorplanning & Architecture design	V	"		
28	13/1/13	Floorplanning method	"	"		
29	14/1/13	Off-chip connections	"	"		
		High level synthesis	"	"		
30	18/1/13	Architecture for low power	"	"		
31	19/1/13	SoC & Embedded CPU	"	"		
32	20/1/13	Architecture testing	"	"		
33	26/1/13	Introduction to CAD systems (algorithms) & Chip design	VI	Blackboard		
34	21/1/13	Layout synthesis & Layout Analysis	"	"		
35	24/1/13	Scheduling & Budget	"	"		
36	28/1/13	Hardware/Software	"	"		

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		Co-design	VI	Blackboard		
37	29/1/13	chip design methodology	"	"		
38	3/1/13	A simple design example	"	"		
39	1/1/13	Revision	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100	"		
40	4/1/13	Revision	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100	"		